IN THE SPECIFICATION

Page 11, paragraph beginning on line 8:

The measurements with respect to Figures 1-7 are not polarity specific. Thus, for example, as illustrated in Figure 8, the capacitance between the gate 50 and the drain 44 may be measured using the present method wherein the drain 44 is connected to the sense terminal T_S while the gate ~~40~~ 50 is connected to the bias terminal T_B. The source 42 and the well 46 are connected to the guard terminal T_G which is at the same potential as the sense terminal T_S connected to drain 44.

Page 15, paragraph beginning on line 6:

Figure 15 illustrates a measuring pad 83 connected to the bit line 82. A pair of guard or shield strips 87B are provided adjacent the pad 83B on the same plane or interconnect level. A shield plate 89B is provided below the pad 83B and the shield strips 87B at a different level to segregate the pad 83B for the remainder of the integrated circuit. The shield strips 87B and the pad 89B are connected to the guard terminal T_G to isolate the pad 83 and prevent it from affecting or creating any parasitic capacitance in the integrated circuit during the testing. The structures 83B, 87B and 89B are provided on the integrated circuit for tests or measurement purposes. The arrows indicate independent connections for the capacitor cell plate 86P, word line 84P, the body bulk or well region 96P and the neighboring word line 82P.